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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/919,372	07/31/2001	Vadim Gutnik	5347-205	2525

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EXAMINER
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CHUNG, PHUNG M

ART UNIT	PAPER NUMBER
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2133

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/919,372

Applicant(s)

GUTNIK ET AL.

Examiner

Phung My Chung

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 07 April 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-26 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

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1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1, 6, 14, 18-19 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Doblar et al (6,516,422).

As per claim 1, Doblar et al disclose the invention substantially as claimed, comprising:

a first clock circuit that is configured to generate a first clock signal responsive to an error signal;

a second clock circuit that is configured to generate a second clock signal responsive to the error signal (see col. 6, lines 18-57); and

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a phase detector circuit that connects the first clock circuit to the second clock circuit and is configured to generate the error signal responsive to the first and the second clock signals (col. 4, lines 18-24).

As per claim 6, the teaching of Doblar et al had been discussed above. The following circuits are inherent in system of Doblar et al: a first pulse generator circuit that is configured to generate a first pulse signal responsive to the first clock signal;

a second pulse generator circuit that is configured to generate a second pulse signal responsive to the second clock signal; and

an arbiter circuit that is configured to generate the error signal responsive to the first pulse signal and the second pulse signal. (See col. 7, line 38 to line 6 of col. 8 and col. 8, line 63 to line 7 of col. 9).

As per claim 14, this method claim is also rejected under the same rationale as set forth in the system claim 1.

As per claim 18, this claim is also rejected under the same rationale as set forth in claim 6.

As per claim 19, this claim is also rejected under the same rationale as set forth in claim 1.

As per claim 23, this claim is also rejected under the same rationale as set forth in claim 6.

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3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 2-3, 7-9, 12-13, 15-16, 20-21 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doblar et al (6,516,422).

As per claim 2, the teaching of Doblar et al had been discussed above. Doblar et al do not disclose: a third clock circuit that is configured to generate a third clock signal responsive to a second error signal; and

a second phase detector circuit that connects the first clock circuit to the third clock circuit and is configured to generate the second error signal responsive to the first and the third clock signals;

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wherein the first clock circuit is further configured to generate the first clock signal responsive to the first and the second error signals. However, Doblar et al (col. 4, lines 18-24 and col. 6, lines 30-37) already disclose the first phase detector circuit connected to the first and second clock circuits and is configured to generate the error signal responsive to the first and the second clock signals. Therefore, it would have been a matter of design choice to a person of ordinary skill in the art, at the time the invention was made, to set a third clock circuit configured to generate a third clock signal responsive to a second error signal; and

a second phase detector circuit that connects the first clock circuit to the third clock circuit and is configured to generate the second error signal responsive to the first and the third clock signals, wherein the first clock circuit is further configured to generate the first clock signal responsive to the first and the second error signals as desired if needed.

As per claim 3, the teaching of Doblar et al had been discussed above. Doblar et al further disclose:

a loop filter circuit (416) that is configured to generate a control signal at an output terminal thereof; and

an oscillator (418) that is configured to generate the first clock signal responsive to the control signal. (See col. 1, lines 26-28 and col. 6, lines 47-49).

As per claim 8, this claim is also rejected under the same rationale as set forth in claims 1 and 2.

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As per claim 9, the teaching of Doblar et al had been discussed above. Doblar et al do not disclose a plurality of loop filter circuits and a plurality of oscillator circuits. However, Doblar et al do teach a loop filter circuit and an oscillator circuit. (See col. 1, lines 26-28 and col. 6, lines 47-49). Therefore, it would have been a matter of design choice to a person of ordinary skill in the art, at the time the invention was made, to set more than one loop filter circuits and more than one oscillator circuit as desired if needed. This is because Doblar et al already disclose at least one filter circuit and at least one oscillator circuit.

As per claim 12, the teaching of Doblar et al had been discussed above. The following circuits are inherent in the system of Doblar et al: a first pulse generator circuit that is configured to generate a first pulse signal responsive to the first clock signal;

a second pulse generator circuit that is configured to generate a second pulse signal responsive to the second clock signal; and

an arbiter circuit that is configured to generate the error signal responsive to the first pulse signal and the second pulse signal. (See col. 7, line 38 to col. 8, line 6 and col. 8, line 63 to line 7 of col. 9). Doblar et al do not disclose a plurality of first pulse generator circuits; a plurality of second pulse generator circuits and a plurality of arbiter circuits. However, it would have been a matter of design choice to a person of ordinary skill in the art, at the time the invention was made, to set more than one first pulse generator circuits, more than one second pulse generator circuits and more than one arbiter circuits as desired if need. This is because Doblar et al already disclose at least one pulse generator circuit and at least one arbiter circuit.

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As per claims 15-16 and 20-21, these claims are also rejected under the same rationale as set forth in claim 2.

As per claims 7, 13 and 24, the teaching of Doblar et al had been discussed above. They do not specifically disclose that wherein the first clock circuit, the second clock circuit and the phase detector circuit are contained in a single integrated circuit chip. However, it would have been a matter of design choice to a person of ordinary skill in the art, at the time the invention was made, to use a single integrated circuit chip for the first clock circuit, the second clock circuit and the phase detector circuit as desired if needed.

5. Claim 4-5, 10-11, 17 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doblar et al (6,516,422) further in view of Barrett, Jr. et al (5,644,743).

As per claim 4, the teaching of Doblar et al had been discussed above. Doblar et al do not disclose a summation circuit that is configured to add the first and second error signals to generate a composite error signal. However, Barrett, Jr. et al disclose phase error detectors for detecting phase errors between first and second clocks signal and a summation circuit that is configured to add the first and second error signals to generate a composite error signal. (See Fig. 1, col. 4, lines 32-40). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention, to incorporate the summation circuit of Barrett, Jr. et al into the invention of Doblar et al to combine the first and second error signals to generate a composite control signal representing the phase error.



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As per claim 5, the teaching of Doblar et al and Barrett, Jr. et al had been discussed above. Doblar et al further disclose wherein the loop filter circuit comprises an operational amplifier circuit that is responsive to the error signal (col. 4, lines 28-33). Dolar et al and Barrett, Jr. et al do not disclose a second amplifier circuit that is responsive to the composite error signal and is connected to the first amplifier circuit at the output terminal. However, it would have been a matter of design choice to a person of ordinary skill in the art, at the time the invention was made, to set another amplifier circuit connected to the first amplifier circuit in responsive to the composite error signal at the output terminal as desired if needed.

As per claim 10 this claim is also rejected under the same rationale as set forth in claim 4.

As per claim 11, this claim is also rejected under the same rationale as set forth in claim 5.

As per claim 17 and 22, these claims are also rejected under the same rationale as set forth in claim 4.

6. Claims 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doblar et al (6,516,422) in view of Van De Graaff (6,822,925).

As per claim 26, Doblar et al disclose the invention substantially as claimed, comprising:  
a means for independently generating a plurality of clock signals on an integrated circuit;  
and a phase detector is configured to produce a phase error signal indicative of the difference between the clock signals (See col. 4, lines 18-24 and col. 6, lines 18-23). Doblar et al do not

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disclose a means for synchronizing phases of the plurality of clock signals to one another based on error signals that are generated based on relative phase difference between ones of the plurality of clock signals. However, Van De Graaff discloses a clock skew adjustment circuit to provide a synchronous clock for the circuit based on error signals. (See col.1, lines 59-65 and col. 9, lines 58-61). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the clock skew adjustment to provide synchronous clock for the circuit as taught by Van De Graaff into the invention of Doblar et al to reduce clock period matching, or lock times, in integrated circuits with clock skew adjustment circuits and reduced overall circuit size.

As per claim 25, this method claim is also rejected under the same rationale as set forth in system claim 26.

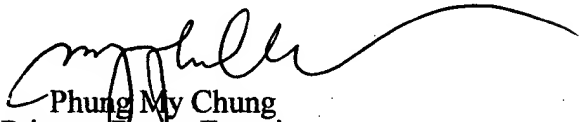
7. Applicant's arguments with respect to claims 1-26 have been considered but are moot in view of the new ground(s) of rejection.

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8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phung My Chung whose telephone number is 571-272-3818. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571- 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Phung My Chung  
Primary Patent Examiner